

**REMARKS**

Claims 1 through 4 and 6 through 31 are currently pending in the application.

This amendment is in response to the final Office Action of February 20, 2003.

Claims 1 through 4 and 6 through 8 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 4 and 6 through 8 of U.S. Patent 6,221,753 in combination with U.S. Patent 5,981,314 to Glenn.

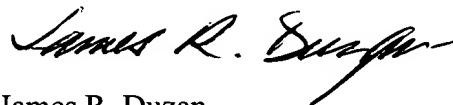
Claims 9 through 31 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 9 through 31 of U.S. Patent 6,221,753 in combination with U.S. Patent 4,612,083 to Yasumodo.

In order to avoid further expenses and time delay, Applicant elects to expedite the prosecution of the present application by filing a terminal disclaimer to obviate the double patenting rejections in compliance with 37 C.F.R. §1.321 (b) and (c). Applicant's filing of the terminal disclaimer should not be construed as acquiescence of the Examiner's double patenting or obviousness-type double patenting rejection. Attached is the terminal disclaimer and accompanying fee.

Claims 1, 9, 17 and 25 have been amended for the sake of clarity.

Applicant request the allowance of claims 1 through 4 and 6 through 31 and the case passed for issue.

Respectfully submitted,



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JRD/sls:djp

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

1. (Twice amended) An assembly method for a semiconductor assembly, comprising:

providing a first substrate having a facing surface and having at least one lead having a portion thereof located on said facing surface of said first substrate, said at least one lead having at least one conductive pad disposed on the portion thereof located on said facing surface of said first substrate, said at least one conductive pad of said at least one lead of said first substrate having a thickness and having a contact surface area;

providing a second substrate having a facing surface and having at least one lead having a portion thereof located on said facing surface of said second substrate, said at least one lead having at least one conductive pad disposed on the portion thereof located on said facing surface of said second substrate, said at least one conductive pad of said at least one lead of said second substrate having a thickness and having a contact surface area;

providing a passivation layer on said facing surface of said first substrate, said passivation layer having a thickness greater than said thickness of said at least one conductive pad of said at least one lead of said first substrate such that said at least one conductive pad of said at least one lead of said first substrate is recessed a distance within [an opening of ]said passivation layer;

forming an opening in said passivation layer at the location of said at least one conductive pad of said at least one lead of said first substrate;

attaching said first substrate to said second substrate, said at least one conductive pad of said at least one lead of said second substrate extending a distance within [an]said opening[ of] in said passivation layer of said first substrate;

abutting said contact surface area of said at least one conductive pad of said at least one lead of said first substrate against said contact surface area of said at least one conductive pad of said at least one lead of said second substrate;

forming direct sliding movable contact between said contact surface area of said at least one conductive pad of said at least one lead of said first substrate and said contact surface area

of said at least one conductive pad of said at least one lead of said second substrate, and establishing electrical communication therebetween; and encapsulating said first substrate and said second substrate with an encapsulation material.

9. (Twice amended) An assembly method for a semiconductor assembly, comprising:

providing a first substrate having a first surface and having at least one lead having a portion thereof located on said first surface of said first substrate, said at least one lead having at least one conductive pad disposed on said portion thereof located on said first surface of said first substrate, said at least one conductive pad of said at least one lead of said first substrate having a substantially flat surface area and having a thickness;

providing a second silicon substrate having a first surface and having at least one lead having a portion thereof located on said first surface of said second substrate, said at least one lead having at least one conductive pad disposed on said portion thereof located on said first surface of said second substrate, said at least one conductive pad of said at least one lead of said second substrate having a substantially flat surface area and having a thickness;

providing a passivation layer on said first surface of said first substrate, said passivation layer having a thickness greater than said thickness of the at least one conductive pad of said at least one lead of said first substrate, said at least one conductive pad of said at least one lead of said first substrate being recessed a distance within [an opening of] said passivation layer;

forming an opening in said passivation layer at the location of said at least one conductive pad of said at least one lead of said first substrate;

attaching said first substrate to said second substrate, said at least one conductive pad of said at least one lead of said second substrate extending a distance within [an said opening[ of] in said passivation layer of said first substrate; and

abutting said flat surface area of said at least one conductive pad of said at least one lead of said first substrate against said flat surface area of said at least one conductive pad of said at least one lead of said second substrate; and

forming a direct sliding movable contact between said flat surface area of said at least one conductive pad of said at least one lead of said first substrate and said flat surface area of said at least one conductive pad of said at least one lead of said second substrate, and establishing electrical communication therebetween.

17. (Twice amended) An assembly method for a semiconductor assembly, comprising:

providing a first silicon substrate having a plurality of leads on a first surface thereof, each lead of said plurality of leads of said first substrate having a conductive pad disposed thereon in substantially a horizontal plane, each conductive pad of said first substrate having a substantially flat surface area and having a thickness;

providing a second substrate having a plurality of leads on a first surface thereof in a substantially horizontal plane, each lead of said plurality of leads of said second substrate having a conductive pad disposed thereon, each conductive pad of said second substrate having a substantially flat surface area and having a thickness;

providing a passivation layer on said first surface of said first substrate, said passivation layer having a thickness greater than said thickness of each conductive pad of said first substrate, each said conductive pad of said first substrate being recessed a distance within [an opening of ]said passivation layer;

forming an opening in said passivation layer at the each location of said each conductive pad of said first substrate;

attaching said first substrate to said second substrate, each said conductive pad of said second substrate extending a distance within [an]said opening [of ]in said passivation layer of said first substrate; and

abutting said flat surface area of said each conductive pad of said first substrate against said flat surface area of one said conductive pad of said second substrate; and

forming a direct sliding movable contact between said flat surface area of said each conductive pad of said first substrate and said flat surface area of one said conductive pad of said second substrate, and establishing electrical communication therebetween.

25. (Twice amended) An assembly method for a semiconductor assembly, comprising:

providing a first silicon wafer substrate having a plurality of leads on a first surface thereof, each lead of said plurality of leads of said first silicon substrate having a conductive pad disposed on a portion thereof in substantially a horizontal plane, each conductive pad of said first silicon substrate having a substantially flat surface area and having a thickness;

providing a second silicon substrate having a plurality of leads on a first surface thereof in a substantially horizontal plane, each lead of said plurality of leads of said second silicon substrate having a conductive pad disposed thereon, each conductive pad of said second silicon substrate having a substantially flat surface area and having a thickness;

providing a passivation layer on said first surface of said first silicon substrate, said passivation layer having a thickness greater than said thickness of each said conductive pad of said first silicon substrate, each said conductive pad of said first silicon substrate being recessed a distance within [an opening] of said passivation layer;

forming an opening in said passivation layer for said each conductive pad of said first silicon substrate;

attaching said first silicon substrate to said second silicon substrate, each said conductive pad of said second silicon substrate extending a distance within [an] said opening [of] in said passivation layer of said first silicon substrate; and

abutting said flat surface area of said each conductive pad of said first silicon substrate against said flat surface area of one said conductive pad of said second silicon substrate; and

forming a direct sliding movable contact between said flat surface area of said each conductive pad of said first silicon substrate against said flat surface area of one said conductive pad of said second silicon substrate, and establishing electrical communication therebetween .

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE SPECIFICATION:**

A marked-up version of paragraph [0001], highlighting the changes thereto, follows:

[0001] This application is a continuation of application Serial No. 08/788,209, filed January 24, 1997, [pending] now U.S. Patent 6,221,753, issued April 24, 2001.

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Amended) An assembly method for a semiconductor assembly, comprising:  
providing a first substrate having a facing surface and having at least one lead having a portion thereof located on said facing surface of said first substrate, said at least one lead having at least one conductive pad disposed on the portion thereof located on said facing surface of said first substrate, said at least one conductive pad of said at least one lead of said first substrate having a thickness and having a contact surface area;  
providing a second substrate having a facing surface and having at least one lead having a portion thereof located on said facing surface of said second substrate, said at least one lead having at least one conductive pad disposed on the portion thereof located on said facing surface of said second substrate, said at least one conductive pad of said at least one lead of said second substrate having a thickness and having a contact surface area;  
providing a passivation layer on said facing surface of said first substrate, said passivation layer having a thickness greater than said thickness of said at least one conductive pad of said at least one lead of said first substrate such that said at least one conductive pad of said at least one lead of said first substrate is recessed a distance within an opening of said passivation layer;  
forming an opening in said passivation layer at the location of said at least one conductive pad of said at least one lead of said first substrate;  
attaching said first substrate to said second substrate, said at least one conductive pad of said at least one lead of said second substrate extending a distance within an opening of said passivation layer of said first substrate;

abutting said contact surface area of said at least one conductive pad of said at least one lead of said first substrate against said contact surface area of said at least one conductive pad of said at least one lead of said second substrate; [and]  
forming direct sliding movable contact between said contact surface area of said at least one conductive pad of said at least one lead of said first substrate and said contact surface area of said at least one conductive pad of said at least one lead of said second substrate, and establishing electrical communication therebetween; and  
encapsulating said first substrate and said second substrate with an encapsulation material.

9. (Amended) An assembly method for a semiconductor assembly, comprising:  
providing a first substrate having a first surface and having at least one lead having a portion thereof located on said first surface of said first substrate, said at least one lead having at least one conductive pad disposed on said portion thereof located on said first surface of said first substrate, said at least one conductive pad of said at least one lead of said first substrate having a substantially flat surface area and having a thickness;  
providing a second silicon substrate having a first surface and having at least one lead having a portion thereof located on said first surface of said second substrate, said at least one lead having at least one conductive pad disposed on said portion thereof located on said first surface of said second substrate, said at least one conductive pad of said at least one lead of said second substrate having a substantially flat surface area and having a thickness;  
providing a passivation layer on said first surface of said first substrate, said passivation layer having a thickness greater than said thickness of the at least one conductive pad of said at least one lead of said first substrate, said at least one conductive pad of said at least one lead of said first substrate being recessed a distance within an opening of said passivation layer;  
forming an opening in said passivation layer at the location of said at least one conductive pad of said at least one lead of said first substrate;



attaching said first substrate to said second substrate, said at least one conductive pad of said at least one lead of said second substrate extending a distance within an opening of said passivation layer of said first substrate; and  
abutting said flat surface area of said at least one conductive pad of said at least one lead of said first substrate against said flat surface area of said at least one conductive pad of said at least one lead of said second substrate; and  
forming a direct sliding movable contact between said flat surface area of said at least one conductive pad of said at least one lead of said first substrate and said flat surface area of said at least one conductive pad of said at least one lead of said second substrate, and establishing electrical communication therebetween.

17. (Amended) An assembly method for a semiconductor assembly, comprising:  
providing a first silicon substrate having a plurality of leads on a first surface thereof, each lead of said plurality of leads of said first substrate having a conductive pad disposed thereon in substantially a horizontal plane, each conductive pad of said first substrate having a substantially flat surface area and having a thickness;  
providing a second substrate having a plurality of leads on a first surface thereof in a substantially horizontal plane, each lead of said plurality of leads of said second substrate having a conductive pad disposed thereon, each conductive pad of said second substrate having a substantially flat surface area and having a thickness;  
providing a passivation layer on said first surface of said first substrate, said passivation layer having a thickness greater than said thickness of each conductive pad of said first substrate, each said conductive pad of said first substrate being recessed a distance within an opening of said passivation layer;  
forming an opening in said passivation layer at the each location of said each conductive pad of said first substrate;

attaching said first substrate to said second substrate, each said conductive pad of said second substrate extending a distance within an opening of said passivation layer of said first substrate; and  
abutting said flat surface area of said each conductive pad of said first substrate against said flat surface area of one said conductive pad of said second substrate; and  
forming a direct sliding movable contact between said flat surface area of said each conductive pad of said first substrate and said flat surface area of one said conductive pad of said second substrate, and establishing electrical communication therebetween.

25. (Amended) An assembly method for a semiconductor assembly, comprising:  
providing a first silicon wafer substrate having a plurality of leads on a first surface thereof, each lead of said plurality of leads of said first silicon substrate having a conductive pad disposed on a portion thereof in substantially a horizontal plane, each conductive pad of said first silicon substrate having a substantially flat surface area and having a thickness;  
providing a second silicon substrate having a plurality of leads on a first surface thereof in a substantially horizontal plane, each lead of said plurality of leads of said second silicon substrate having a conductive pad disposed thereon, each conductive pad of said second silicon substrate having a substantially flat surface area and having a thickness;  
providing a passivation layer on said first surface of said first silicon substrate, said passivation layer having a thickness greater than said thickness of each said conductive pad of said first silicon substrate, each said conductive pad of said first silicon substrate being recessed a distance within an opening of said passivation layer;  
forming an opening in said passivation layer for said each conductive pad of said first silicon substrate;  
attaching said first silicon substrate to said second silicon substrate, each said conductive pad of said second silicon substrate extending a distance within an opening of said passivation layer of said first silicon substrate; and

abutting said flat surface area of said each conductive pad of said first silicon substrate against said flat surface area of one said conductive pad of said second silicon substrate; and forming a direct sliding movable contact between said flat surface area of said each conductive pad of said first silicon substrate against said flat surface area of one said conductive pad of said second silicon substrate, and establishing electrical communication therebetween .